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10/709,004	04/07/2004	Yuan-Kun Hsiao	VOSP0002USA	3003

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EXAMINER	
SINGH, HIRDEPAL	
ART UNIT	**PAPER NUMBER**
2611	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/709,004	HSIAO, YUAN-KUN	
	Examiner	Art Unit	
	Hirdepal Singh	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 August 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *9/30/2007*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Response to Arguments

1. Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

2. Applicant argues that the "Independent claims 1 and 12 have been amended to overcome these claim rejections. Claims 1 and 12 now each recite that the clock generator and clock generating method are applied to a DVD optical drive. Chou does not disclose a clock generator or clock generating method applied to a DVD optical drive. Instead, Chou only discloses in column 1, line 25 and in column 6, line 46 that the optical storage device is a CD-RW drive."

3. In response to applicant's arguments, the recitation "A clock generator being applied to a DVD optical drive..." has not been given patentable weight because the recitation occurs in the preamble. A preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. See *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie*, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951). Therefore, Examiner traverses Applicant's argument as the amended independent claims 1 and 12 recite a DVD optical drive in the preamble, so no patentable weight is given to the recitation. The rejection to claims 1 and 12 still holds.

4. Applicant argues that the "...Chou does not anticipate each and every limitation contained in independent claims 1 and 12, and can no longer be used in a 35 U.S.C. 102(e) rejection. Regarding a potential 35 U.S.C. 103 (a) rejection involving the Chou reference, the applicant would like to point out that Chou and the instant application were commonly owned by VIA Technologies, Inc. at the time that the invention of the instant application was made. The instant application has been assigned to VIA Optical Solution, Inc., which is a subsidiary of VIA Technologies. Therefore, according to 35 U.S.C. 103(c), the Chou reference is disqualified from being used in a 103(a)/102(e) rejection of the claims of the instant application. In light of the common ownership of Chou and the invention of the instant application, reconsideration of claims 1-3, 12, 13, and 15 is respectfully requested."

5. Examiner want to bring this in the Applicant's notice that no official paper (an affidavit etc.), regarding the common assignee of Chou (US 7,016,277) and the instant application, is filed with present amendment to overcome the 35 U.S.C. 102(e) rejection.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1-2, 12-13 and 15 are rejected under 35 U.S.C. 102(e) as being anticipated by Minamino et al. (US 2003/0117915).

Regarding claims 1, 12 and 15:

Minamino et al discloses a clock generator being applied to a DVD optical drive (abstract; paragraphs 0002 and 0042) for generating a non-phase-modulated target clock signal based on a phase-modulated input signal, the clock generator comprising:

an arithmetic/logic circuit for calculating a period count value by counting (413 in figure 4; paragraph 0050) a period of the input signal according to a reference clock having a predetermined frequency, calculating an average value by averaging a plurality of the period count values, and comparing the average value with the period count value for outputting a first control signal; and

a phase-locked loop (paragraph 0007) connected to the arithmetic/logic circuit for generating the target signal according to the first control signal (paragraph 0054-0055 and), and the input signal, feeding the target signal back to the input of the phase-locked loop, and determining whether the target clock signal is to be synchronized with the input signal based on the logic level of the first control signal (paragraphs 0076-0077);

wherein when the first control signal corresponds to a first logic level (paragraph 0076), the phase-locked loop compares the target clock signal with the input signal to drive the target clock signal to be synchronized with the input signal, and when the first control signal corresponds to a second logic level (paragraph 0076), the phase-locked loop holds the target clock signal without driving the target clock signal to be synchronized with the input signal.

Regarding claims 2 and 13:

Minamino et al discloses all of the subject matter as described above and further discloses that the circuit comprises;

reference clock generator generating a reference clock having predetermined frequency (304 in figure 3; paragraph 0049);

a counter connected to reference clock generator counting the number of period according the input or wobble signal (306 in figure 3; paragraph 0050);

a mean or average unit for calculating the average of count number (406 in figure 4; paragraph 0054);

a controller which generates a control signal according to the average value and the rectification value is doing the same function as the comparator in the claimed invention (407 in figure 4; paragraph 0055).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 6, 11, 14, 18 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Minamino et al. (US 2003/0117915).

Regarding claims 6 and 18:

Minamino et al discloses all of the subject matter as described above and further discloses that when the phase difference between signal and encoded sub code frame synchronization signal is a predetermined value the reference clock is the write clock signal (paragraph 0016) except for specifically teaching that when difference between count value and the average value is less than a critical value first control signal is set to a first logic level.

However, it would have been obvious to one of ordinary skill in the art at the time of invention to use the count value and average value of the Minamino device and compare the difference with a predetermined value to decide the logic level of the control signal. One would have been motivated to use the count value and average value to decide the logic level of control signal so that the generated clock signal from the PLL is in the correct phase.

Regarding claims 11 and 20:

Minamino et al discloses all of the subject matter as described above and further discloses that clock generating device may be applied to an optical disc drive as DVD (paragraphs 0002 and 0042), and also discloses that the optical disc recorder simultaneously generate the encoder frame synchronization signal corresponding to each ADIP (paragraph 0016), except for specifically teaching that a second control signal is generated to prohibit the PLL to synchronize the target clock with the input signal at a predetermined time.

However, it is inherent that the absolute timing of the input signal is used to prevent PLL to synchronize the target clock with the input signal at a predetermined time. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to prohibit the PLL from synchronizing the target clock with the input. One would have been motivated not to synchronize the target clock with the input signal at a predetermined time to keep the signal from being unstable.

Regarding claim 14:

Minamino et al discloses all of the subject matter as described above and further discloses generating an average value based on the period count value (paragraph 0054) except for specifically teaching that when average value equals an initial value the comparison between average and count value stops.

However, it is inherent that the average value processor stops comparison with a predefined condition whether it is when the count value becomes equal to the average value.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to generate control signal based on the comparison and stop the comparison as a predefined condition is met. One would have been motivated to use the comparison of average and periods count values to generate the control signal and stop comparing when the period count value equals the average value.

10. Claims 3 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Minamino et al. (US 2003/0117915) in view of Hsu et al. (US 6,754,147).

Regarding claim 3:

Minamino et al discloses all of the subject matter as described above except for specifically teaching that clock generator comprises; a phase detector with wobble signal and the control signal as input and the second synchronization signal as another input, and generating a control signal according to the inputs; the phase detector generating a control voltage for the low pass filter; a voltage controlled oscillator controlling the frequency of the target clock based on the control voltage.

However, Hsu et al in the same field of endeavor discloses a phase locked loop for optical disk drives where the wobble clock generator comprises: a phase detector (12 in figure 6) with wobble signal and the control signal as input and the second synchronization signal as another input, and generating a control signal according to the inputs; the phase detector generating a control voltage (the

phase adjusting ckt. control the phase detector according to ADJ-CTRL control signal) for the low pass filter; a voltage controlled oscillator (18 in figure 6) controlling the frequency of the target clock based on the control voltage.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to use clock generator with a phase detector generating a control voltage and a voltage controlled oscillator controlling the frequency of the target clock based on the control voltage in order to get the out put of the clock generating circuit in a correct phase according to the wobble signal.

Regarding claim 5:

Minamino et al discloses all of the subject matter as described above except for specifically teaching that the clock generating device has a charge pump circuit for controlling the control voltage from the phase detector.

However, Hsu discloses a similar method and device for clock generation and further discloses that the PLL includes charge pump for controlling the voltage based on the phase detection (figure 16; column 1, lines 28-45).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to use a charge pump circuit with the loop filter in the PLL to generate the control voltage in order to use the charge pump included in the PLL circuit to generate the control voltage.

11. Claims 7 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Minamino et al. (US 2003/0117915) in view of Jahene et al. (US 7,039,380).

Regarding claims 7 and 19:

Minamino et al discloses all of the subject matter as described above except for specifically teaching that when difference between plurality of consecutive period count values and the average value are less than a critical value first control signal is set to a first logic level.

However, Jahene et al discloses that when the phase difference is less than a predetermined value the reference clock is the write clock signal (column 2, lines 30-45), and further discloses that the first reference synchronization signal is generated based on the average value of plurality of count values which in turn controls the PLL (figure 5; column 3, lines 56-60).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to use the difference between plurality of consecutive period count values and the average value of the Minamino device and compare the difference with a predetermined value to set the logic level of the control signal. One would have been motivated to set the logic level of control signal according to the difference between plurality of consecutive period count values and the average value to generate clock signal that is in the correct phase.

12. Claims 8-9 and 16-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Minamino et al. (US 2003/0117915) in view of Van Vlerken et al. (US 6,765,861).

Regarding claims 8 and 16:

Minamino et al discloses all of the subject matter as described above except for specifically teaching that when difference between period count value and the average value is larger than a critical value first control signal is set to a second logic level.

However, Van Vlerken et al discloses that when the phase difference is less than a predetermined value the reference clock is the write clock signal (column 2, lines 1-18).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to use the count value and average value and compare the difference with a predetermined value and set the logic level of the control signal to a second logic level if the difference is large or smaller than the predetermined value. One would have been motivated to use the difference between period count value and average value to set the logic level of control signal to a second logic level if the difference is larger than a predetermined value so that the generated clock signal is in the correct phase and does not get altered during the phase modulated cycles of the wobble signal.

Regarding claims 9 and 17:

Minamino et al discloses all of the subject matter as described above except for specifically teaching that when difference between plurality of consecutive period count values and the average value is larger than a critical value first control signal is set to a second logic level.

However, Van Vlerken et al discloses that when the phase difference is less than a predetermined value the reference clock is the write clock signal (column 2, lines 1-18).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to use the count value and average value and compare the difference with a predetermined value and set the logic level of the control signal to a second logic level if the difference is large than the predetermined value. One would have been motivated to use the difference between period count value and average value to set the logic level of control signal to a second logic level if the difference is larger than a predetermined value so that the generated clock signal is in the correct phase and does not get altered during the phase modulated cycles of the wobble signal.

13. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Minamino et al. (US 2003/0117915) in view of Okamoto et al. (US 6,587,417).

Regarding claim 10:

Minamino et al discloses all of the subject matter as described above except for specifically teaching that the clock generating device has a band pass filter.

However, Okamoto discloses a similar method and device for clock generation and further discloses that the device includes a band pass filter and the output of the band pass filter is fed to the level slicer (abstract; figure 13; column 15, lines 20-25).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to use the band pass filter and slicer to select the frequency and level of input signal. One would have been motivated to use the band pass filter and slicer at the input of clock generator to get the controlled input signal with limited amplitude and frequency.

11. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Minamino et al. (US 2003/0117915) in view of Hsu et al. (US 6,754,147) as applied to claim 3 above, further in view of Okamoto et al. (US 6,587,417).

Regarding claim 4:

Minamino et al discloses all of the subject matter as described above except for specifically teaching that the clock generating device has second slicer.

However, Okamoto discloses a similar method and device for clock generation and further discloses that the device includes slice signal processing unit (abstract; figure 14; column 15, lines 20-25).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to use the slicer to select the level of input signal. One would have been motivated to use the slicer in the PLL circuit to get the target signal and input signal having similar waveforms.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hirdepal Singh whose telephone number is 571-270-1688. The examiner can normally be reached on Mon-Fri (Alternate Friday Off)8:00AM-5:00PMEST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Shuwang Liu can be reached on 571-272-3036. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

HS
October 24, 2007

SHUWANG LIU
SUPERVISORY PATENT EXAMINER